Themenliste für das/Topics for
(Haupt)seminar Technische Elektronik
Sommersemester 2017
All topics are offered in German or English

T1: Wear Leveling Techniques for Flash Memories

With its growing density and performance the impact of flash-based mass storage gets bigger and bigger. Hence solid-state drives (SSDs) are commonly used in computer systems these days. Although many new technological innovations made them a reasonable alternative - or even the preferred solution - to traditional electromechanical hard disk drives (HDDs), price issues and reliability and lifetime concerns still inhibit them from replacing their predecessors.
Since the flash cells contained in SSDs can only stand a limited number of write / erase cycles, storage management has to operate differently than it used to with the almost unlimitedly rewritable magnetic disks. Remembering this critical restriction, new techniques have to be developed that allow equal usage of the whole disk space to ensure longer lifetimes.
Familiarize yourself with the concepts of wear leveling and investigate recent techniques presented in literature. Compare them in terms of complexity, performance and applicability to common use cases.

T2: Modeling of Capacitance in Tunneling FETs (in English)

As MOSFETs become smaller, the fundamental limits of CMOS technology make scaling more difficult to achieve. One potential way around these fundamental limits is the Tunneling FET (TFET.) With the TFET, the current flows due to quantum tunneling rather than thermally.

TFETs have many of the same features as MOSFETs, but also some key differences, which allow for better performance in low power applications. Some of these differences are very clear, like the physical structure, but others are not immediately apparent, such as the capacitance. In this seminar, you will look at the differences between a TFET and a MOSFET and how these differences affect how the capacitance in a TFET is modeled differently from a MOSFET.

T3: Time to Digital Converters, a Seminar on Topologies and Specifications of TDCs

Time to Digital Converters (TDC) are an inevitable part of timing specific mixed signal designs. In applications, where the timing of signals is of great interest, TDCs also find their place.
In this seminar you are required to do a research on existing topologies of TDCs, including novel ones. In addition, you get familiar with TDC related specifications. In the final report as well as your final presentation you make a comparison between the topologies and specifications and also discuss possible tradeoffs in the design of TDCs.

T4: Investigation of General Layout Guidelines for RF and MMW ICs using 40nm technology

The Institute for Technical Electronics develops an integrated On-Chip Oscilloscope (OCO) in 40nm CMOS technology, containing a suitable sensor and readout circuitry detecting and characterizing spin-waves in the 5-50 GHz range. Spin wave based devices are one of the promising candidates for beyond-CMOS computing, providing both Boolean and non-Boolean data processing for high-frequency and low power applications. The main challenge of the readout circuitry is the design of components operating in the frequency range of 5-50 GHz.

The task of this seminar is the investigation of general layout guidelines for Radio Frequency (RF) and Millimeter Wave (MMW) circuits using the examples of 40nm technology. First of all, challenges and limits in the layout of RF circuits have to be described and possible solutions proposed. Usage of special RF components like inductors, capacitors, transistors and transmission lines should be explained. Finally, pros and cons of the shrinking transistors in relation to the layout design have to be mentioned.

T5: Effect of Mechanical Stress on Semiconductor Devices

The mechanical stress can occur during the fabrication, assembly and packaging of the integrated circuits. The highest stresses on the silicon surface are the in-plane normal stresses, which cause parametric shifts in the electronic components and lead to a deviation of the circuit parameters from the nominal ones. These parametric shifts are very important by designing of the precision analog and mixed-signal circuits. The effect of the stress can be reduced by designing and choosing of low-stress sensitive electronic devices, but in many systems this approach is not possible (for example MEMs). For this reason, an effective stress compensation circuitry is needed.

In this seminar topic, we want to find out the physical effects causing the parameter shifts of the silicon devices and which electronic components are most susceptible to the stress.
Tasks:

- Understand physics behind piezo effects
    - Sensitivity of different types of resistors, CMOS and Bipolar transistors
    - Sensitivity dependence on crystal
    - Temperature dependence
- Documentation

T6: Room temperature Skyrmions and their applicability for devices

Many state of the art magnetic memory and logic devices in research and industry are based on ultra-thin multilayer ferromagnetic films with perpendicular magnetic anisotropy (PMA), e.g. HDDs, GMR sensors or MRAM. To meet the ever growing demand for more storage and faster data processing in recent years several new effects such as Spin-Hall, Rashba and DMI have been employed to postulate new devices and to propose the significant improvement of current devices' characteristics [1]. The named effects are also a very hot topic in the researchers' community.

One of the most promising phenomenons is skyrmion existence at room temperature enabled by DMI effect. Skyrmions are smallest possible perturbation of a magnet: a point alike region of reversed magnetization, surrounded by a whirling twist of spins [2]. The paper shall give an overview on skyrmion creation manipulation in the PMA magnetic films at room temperature. Furthermore, the applicability of this phenomenon for devices should be discussed. The focus should lie on ultra-thin multilayer films containing at least one of the following materials: Co/CoFeB/Ni.

[1] C. Moreau-Luchaire et al., "Additive interfacial chiral interaction in multilayers for stabilization of small individual skyrmions at room temperature" Nature Nanotechnology 2016, doi:10.1038/nnano.2015.313

[2] C.H. Marrows, "Viewpoint: An Inside View of Magnetic Skyrmions" Physics 8, 40, 2015 online: http://physics.aps.org/articles/v8/40

[3] A. Hellemans. Skyrmions: "Communication With Magnetic Swirls Instead of Electrons" IEEE Spectrum 2014 Online: http://spectrum.ieee.org/nanoclast/semiconductors/nanotechnology/skyrmions-communication-with-magnetic-swirls-instead-of-electrons

[4] D. Johnson, "Developments in Magnetic Skyrmions Come in Bunches Hellemans" IEEE Spectrum 2015 Online: http://spectrum.ieee.org/nanoclast/semiconductors/materials/developments-in-magnetic-skyrmions-come-in-bunches.